Witch Navigator - a software GNSS receiver for education and research

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ABSTRACT

The paper introduces the Witch Navigator, which is an ExpressCard form factor software GNSS receiver for a notebook or a personal computer, developed for educational and research purposes. The signal processing runs on a FPGA and a PC processor, the mutual communication is realized via a PCI Express bus. The receiver is equipped with two reconfigurable front ends. The complex multi-antenna, multi-frequency and multi-constellation GNSS system can be built by interconnecting several receiver cards by a special connector. The receiver can operate in a classical mode with hardware GNSS correlators which are programmed into the FPGA, or in a pure processor mode in which the PC processor directly processes signal samples measured by the receiver in real time. For the processing of most of the GNSS signals, the universal GNSS correlator has been developed and tested. The FPGA signal processor is equipped with a signal capture unit for the measurement of the signal snapshots for the DSP signal acquisition in the PC. The processing of the extremely wideband GNSS signals (Galileo E5) is realizable by a special method the performance of which is only slightly poorer than the performance of the optimum receiver, while the hardware complexity is a quarter of the optimum one.

KEYWORDS: Software GNSS receiver, Galileo E5, ExpressCard, GNSS correlator

1. INTRODUCTION
The GNSS is a rapidly developing branch that requires high quality experts, scientists and specialists. The first rate education requires not only deep theoretical training, but also practical experiments with the GNSS signal processing. Postgraduate students should be educated in the development, implementation and testing of new non-standard signal processing algorithms used in special scientific applications. The price of such education and training is very important especially in times of economic crisis. The Witch Navigator project is a project of the software GNSS receiver for education and research. The major aims of the Witch Navigator project are:

- design and programming of an open source GNSS receiver capable to process most of the civil GNSS signals,
- high performance but low cost signal processor and receiver hardware,
- capability to process signals on several frequencies and from several antennas,
- free of charge but user friendly development tools.

These contradictory design requirements have led to the use of a notebook or PC workstation for signal processing purposes. The receiver is designed as an ExpressCard periphery (Figure 1) for the computer. The PC or notebook platforms were chosen due to their low cost, high computing power and easy to use development tools for the signal processing and receiver control implementation. The receiver is designed to be able to employ the traditional receiver concept with FPGA correlators or pure processor signal processing in which all signal processing including the correlation reception runs on the PC. This concept gives an application developer the opportunity to implement signal processing algorithms in different ways or combine several methods or choose the most convenient one. For instance, the high computing power enables to implement parallel DSP signal acquisition algorithms which reduces the acquisition time, shortens the receiver’s time to the first fix and increases its sensitivity.

![Figure 1. Witch Navigator](image)

The crucial part of the Witch Navigator receiver is the FPGA configuration and the PC
software. The software is designed universally. The predominant part (70%) of the software code is independent of the GNSS system and signal. This approach facilitates the implementation of the signal processing of the particular GNSS systems and signals.

2. Receiver hardware

The hardware part of the Witch Navigator is a standard ExpressCard computer periphery (Figure 2) equipped with two programmable front ends (Kovář et al., 2009) and a FPGA signal processor which communicates with the PC via the PCI Express bus. The PCI Express bus is characterized by the wide data throughput and low latency. Our receiver therefore enables to implement different types of the GNSS receiver architectures:

- the traditional architecture, which utilizes the “hardware” signal processor for processing the navigation signals and
- a receiver architecture with pure microprocessor signal processing in the PC CPU and the GPU or
- a mixed architecture (combination of the two previous ones)

The Witch Navigator hardware is designed on a single six-layer printed circuit board. The board is housed in an aluminium shield.

The receiver is equipped with two expansion connectors K6 and K7 (see Figure 1), which enable

- to interconnect several cards by the ribbon cable to the complex multi frequency and multi antenna receiver
- to connect external high precise clock standard
- to connect external sensors (INS, odometer, altimeter, RF front end for the processing of the other terrestrial navigation and communication signals etc.)
- to attach a GNSS signal modulator for the generation of the GNSS signal or to replay the recorded GNSS signals

The GNSS antennas are connected via the antenna connectors K1 and K2. The low cost GPS
L1 active antenna can be used for GPS L1 or Galileo E1 signals. The reception of the complex GNSS signals requires a specialized active antenna with the built-in RF filter.

3. GNSS signal processor

The GNSS signal processor, which is fully reconfigurable, is programmed to the FPGA. The user can either implement a specific (optimum) signal processing algorithm for a given GNSS signal or use a universal signal processor (Kovář et al., 2010), designed for the processing of most of the GNSS signals. We chose the latter, as it speeds up and simplifies the development of a GNSS receiver in spite of the non-optimality in the processing of certain GNSS signals. The block diagram of the FPGA configuration is in Figure 3. The core of the FPGA signal processor is the Universal GNSS Correlator (Figure 4), which is the FPGA resources optimized implementation of the GNSS correlator capable to process most of the civil GNSS signals. The Universal GNSS Correlator is extended with the real-time signal capture unit capable to send a signal sample to the computer for further processing.

The remaining blocks of the FPGA serve for the communication via the PCI Express bus and a configuration of the front ends via the I2C bus.

The Universal GNSS Correlator supported signals are specified in Table 1. The Universal GNSS Correlator can also directly process signals of the augmentation systems like WAAS, EGNOS and QZSS etc. on L1 and L5 frequencies.

According to the preliminary information Hein (2006), Gibons (2008) and Gao et al. (2007) of the Compass signal, the Universal GNSS Correlator and the Witch Navigator receiver are capable to process the Compass signals including the high-precise joined processing of the signals spectrally distributed under and above L1 frequency by a method similar to the method proposed in the chapter 5.2.

![Figure 3. FPGA processor block diagram](image)
Table 1. Signals supported by the Universal GNSS Correlator

<table>
<thead>
<tr>
<th>System</th>
<th>Signal</th>
<th>Support</th>
<th>Universal correlators number</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPS</td>
<td>L1 C/A</td>
<td>YES</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>L2 CA</td>
<td>Partially</td>
<td>1</td>
<td>Data channel only</td>
</tr>
<tr>
<td></td>
<td>L5</td>
<td>YES</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>L1C</td>
<td>Partially</td>
<td>2</td>
<td>BOC(1,1) component only</td>
</tr>
<tr>
<td>GLONASS</td>
<td>L1</td>
<td>YES</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>L2</td>
<td>YES</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>GALILEO</td>
<td>E1b</td>
<td>YES</td>
<td>1</td>
<td>BPSK method, BOC(6,1) component is not considered, tested</td>
</tr>
<tr>
<td></td>
<td>E1c</td>
<td>YES</td>
<td>1</td>
<td>BPSK method, BOC(6,1) component is not considered, tested</td>
</tr>
<tr>
<td></td>
<td>E5</td>
<td>YES</td>
<td>4</td>
<td>Two QPSK sub-carriers</td>
</tr>
<tr>
<td></td>
<td>E5a</td>
<td>YES</td>
<td>2</td>
<td>Tested</td>
</tr>
<tr>
<td></td>
<td>E5b</td>
<td>YES</td>
<td>2</td>
<td>Tested</td>
</tr>
</tbody>
</table>

4. Software

The PC software (Figure 5) has been designed for all three receiver architectures – a pure microprocessor signal processing architecture, the traditional architecture and their combination (mixed architecture). The implementation of the pure microprocessor architecture comprises a continual unidirectional transfer of the signal samples from the receiver to the computer via the PCI Express bus, whereas the traditional architecture requires a strictly real-time receiver handling and a bidirectional data transfer.
The implementation of the former architecture comprises a continual reception of the sample blocks into the PC memory and the sequential processing of them. If strictly non-real-time results are needed, the blocks can be grouped and processed at once in order to ease the system scheduling requirements. The computer processing then includes the signal acquisition, tracking, data synchronization, decoding, and position, velocity and time (PVT) estimation.

The mixed architecture for instance performs the acquisition on the PC itself, whereas the tracking loops are closed over the FPGA and the PC. Consequently, the high-rate sample blocks must be transferred to the PC, as well, and a real-time (RT) bidirectional communication must be established. In this text, we pay attention to the implementation of the mixed architecture, since its modification towards the pure processing architecture and the traditional architecture is straightforward. Due to the high-rate data transfer of the signal snapshots, direct memory access (DMA) from the FPGA to the PC had to be implemented.

The FPGA (Master) generates an interrupt every time the data transfer to the PC (Slave) is finished. The PC then handles the interrupt, calculates the updated values and transmits the data back on the bus. The time relation between two adjacent data transfers is depicted in Figure 6. TIC denotes the instant of increment of the time interval counter which is coincident with the commencement of the DMA transfer. The transfer in the opposite direction was implemented as the PCI Express Memory Write for simplicity.
In this project, we selected a soft real-time OS (RTOS) in the form of a Linux OS with the RT Pre-emptive Patch developed by the group of Linux kernel programmers. The key advantages of this selection are:

- no extra RT application programming interface (API) is needed,
- the Linux OS with the RT Pre-emptive Patch is an open source project,
- the installation of the OS can be accomplished by patching any standard (vanilla) Linux kernel,

The example of the Witch Navigator program user interface is in Figure 7. The user interface serves for receiver control and monitoring. The individual screens display basic operation parameters concerning the receiver hardware operation and setup, such as the front ends’ status. The user can monitor the kernel driver operation, PCI express communication and interrupt dropouts. The next screen displays the navigation data, such as the user PVT, satellite constellation, and the receiver channels status.

The first application is of course the implementation of the GPS L1 signal processing. We work on the implementation of the dual frequency GLONASS receiver and Galileo E1 and E5a&b and E5 economical receiver (it is described below). The other signal processing will follow in the near future. We plan to implement some signal processing to the multi core GPU, for instance the GNSS signal acquisition.
5.1 GPS L1

This paragraph summarizes some results of the implementation of the GPS L1 signal processing. The current GPS L1 application utilizes the standard signal processing except the DSP signal acquisition and the narrow correlator. No other special signal processing methods, like high sensitivity and multipath mitigation techniques are programmed. This application serves for the Witch Navigator concept testing and as a starting point (example implementation) for the implementation of the other GNSS signals. Let us notice that the processing of the modernized and new GNSS signals consists of similar parts as the GPS L1 processing, i.e. signal acquisition and signal tracking. The correlator handling runs also on the same period. The differences are in the frequency and the Universal GNSS Correlator configuration, the replica waveform in the DPS acquisition and the navigation message structure.

The GPS L1 application for the Witch Navigator was tested with the Spirent signal simulator. Some of the results are in Figure 8.

**Figure 8.** GPS L1 test results: a) 3D position error, b) 2D position error plot, c) 3D velocity error, d) 2D velocity error plot
5.2 GALILEO E5

This paragraph outlines the implementation of the signal processing of the Galileo E5 signal into the Universal GNSS Correlator and the Witch Navigator receiver. The problem of the Galileo E5 signal is its extreme bandwidth, approximately 90 MHz. The signal processor, which implements the correlation reception (Kačmářík et al., 2008) has to run on an extremely high sampling frequency and thus the hardware complexity and power consumption are very high. Fortunately, the cross-correlation function of the complete E5 signal, which is required for the implementation of the correlation reception techniques, can be calculated from the cross-correlation function of E5a and E5b signal components (1). The calculation respects the phase relationship between E5a and E5b sub-carriers. Both E5a and E5b correlators must be jointly controlled as shown in Figure 9.

\[
R_{mE5}(\tau) = e^{j2\pi f_{x,sc} \tau} \int \left( e_{E5a-1}(t) + j.e_{E5a-Q}(t) \right) \left( e_{E5a-1}(t + \tau) - j.e_{E5a-Q}(t + \tau) \right) dt + e^{-j2\pi f_{x,sc} \tau} \int \left( e_{E5b-1}(t) + j.e_{E5b-Q}(t) \right) \left( e_{E5b-1}(t + \tau) - j.e_{E5b-Q}(t + \tau) \right) dt = e^{j\phi} e^{j2\pi f_{x,sc} \tau} R_{E5a}(\tau) + e^{j\phi} e^{-j2\pi f_{x,sc} \tau} R_{E5b}(\tau) \tag{1}
\]

The first summand of (1) can be measured by the E5a correlator and the second one by the E5b correlator independently.

For the realization of the standard GNSS delay discriminators usually the early (E) and late (L) values or values for other time shifts of the cross-correlation between the received signal and the replica are needed. These values can be calculated in the vicinity of the cross-correlation maximum from the prompt \(P_A\) and \(P_B\) measurements of E5a and E5b correlators’ outputs by the formulas

\[
E = e^{-j\phi} e^{-j\omega_\Delta \tau} P_A + e^{j\phi} e^{j\omega_\Delta \tau} P_B,
\]

\[
L = e^{j\phi} e^{j\omega_\Delta \tau} P_A + e^{-j\phi} e^{-j\omega_\Delta \tau} P_B, \tag{2}
\]

where \(\Delta\) is a correlator spacing.

The Galileo E5 signal receiver based on the formulas (2) we termed the receiver using the optimum E5 correlator. It is so because of the lower sampling frequency and simplicity of the partial E5a and E5b correlators.

The proposed E5 signal processing concept, briefly described above, was tested by the computer simulation (Figure 10) and compared with the optimum E5 receiver, E5a and E5b receiver and a receiver which combines the independent E5a and E5b measurements (E5a&E5b). The performance of the ecoE5 receiver is only slightly poorer than the performance of the optimum E5 receiver. The small precision losses are caused by the omitting of the auxiliary components of the E5 signal which compensates the signal envelope and by other simplifications. The detailed description of our algorithm of Galileo E5 signal...
processing will be published in the near future.

The algorithm can be simply modified to the reception of signals of other systems which use similar modulations, e.g. Compass.

Figure 9. Block diagram of the ecoE5 receiver

Figure 10. Performance comparison of the E5 signal processing
6. Conclusions

The Witch Navigator receiver is a universal GNSS receiver, which can be used for the education and research of the GNSS. The user can also use it for the development, implementation and testing of signal processing algorithms. The user has full control over the receiver hardware and software. By interconnecting several Witch Navigator cards it is possible to build multi-frequency, multi-antenna and multi-constellation receiver processing simultaneously a large number of the GNSS signals. Such a receiver can have specific properties suitable for many applications, i.e. very high precision of the PVT determination.

The Witch Navigator can be integrated with external sensors (i.e. INS or another RNAV system) by means of the expansion connectors.

The receiver is capable to process wideband GNSS signals with BOC type modulation by the economical method, see par. 5.2.

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REFERENCES


Hein G (2006) GNSS Interoperability: Archiving of Global System of Systems or “Does everything Have to be the Same “, InsideGNSS Jan/Feb 2006, 57-60

