User Guide

Witch Navigator FPGA Processor

FPGA v. 1.0 Programming Interface

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Pavel Kovář

Witch Navigator

FPGA Processor Ver. 1.0

Date	Version	Revision
14/10/2010	1.0	Witch Navigator FPGA Processor 1.0 release

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Nomenclatures

ADC	Analog to Digital Converter
AltBOC	Alternate BOC
BOC	Binary Offset Carrier modulation
C/A	Coarse/Acquisition
DMA	Direct Memory Access
DW	Data Word
FPGA	Field-Programmable Gate Array
GLONASS	GLObalnaja NAvigacionna Sputnikovaja Sistema
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
Irq	Interrupt
LED	Light-Emitting Diode
LSB	Least Significant Byte
MSB	Most Significant Byte
MSI	Message Send Interrupt
NCO	Numerically Controlled Oscillator
PCIe	PCI Express Interface
PCIeIIP	PCI Express Interface IP
PLL	Phase Lock Loop
PRN	Pseudo Random Noise
UCorIP	Universal Correlator IP
TIC	Time Interval Counter
VHDL	Very High speed integrated circuit hardware Description Language
WNAV	Witch NAVigator

1 Introduction

The Witch Navigator FPGA Processor Programmer Guide describes the software control of the FPGA processor. The organization of the document comes out from the block diagram of the FPGA processor in Figure 1. The key part of the FPGA processor is the Universal Correlator IP (UCorIP) which processes the GNSS signals. Besides this, the UCorIP implements input and output memory registers not only for UCorIP itself, but also for the other blocks. Addressing of these registers are therefore described in the chapter concerning the Universal Correlator IP, but the description and function of the other blocks can be found in separate chapters.

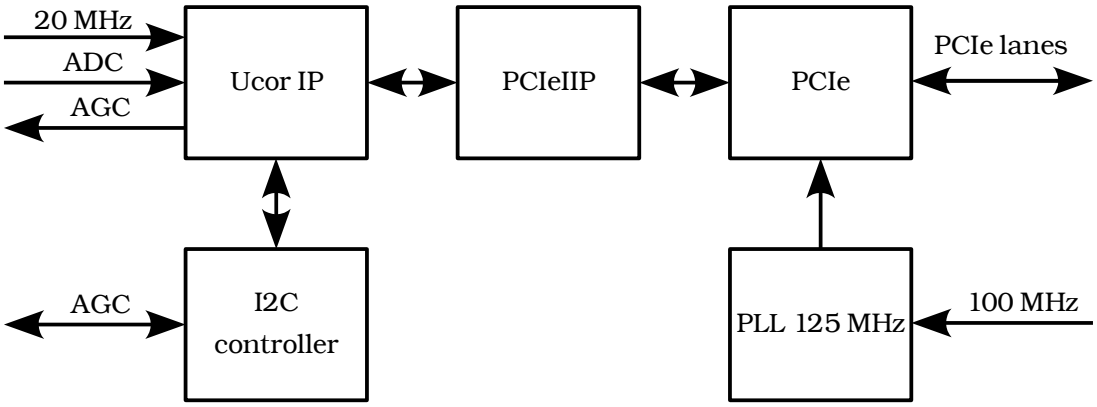

Figure 1: Witch Navigator FPGA pocessor

2 Universal Correlator IP

The Universal Correlator IP (UCor) is an *FPGA-resource-economic implementation of the classical E-L correlator* for GNSS signal processing and a *signal-samples capture unit* at the same time (Figure 2). The structure of the universal correlator was optimized for processing most of the GNSS signals:

- GPS L1 C/A
- GPS L2 C/A data channel
- WAAS, EGNOS
- GPS L5
- GLONASS
- Galileo E5

- Galileo E5a, E5b
- Galileo E 1b, E 1c

The universal correlator consists of *24 simple E-L correlators* (Figure 3) with RAM-based PRN generators with the *maximal length of 10230 chips* and with a *controlled correlator space*. This correlator can directly process BPSK modulated GNSS signals like GPS L1 C/A, WAAS/EGNOS or GLONASS, for example. Two correlators are needed for processing of the QPSK signals like GPS L5, Galileo E5a or E5b. The processing of Galileo E5 AltBOC modulated signal by four universal correlators is described in [1]. The BOC signals can be understood as special cases of the BPSK modulated signals with a modification of their PRN code rates. Hence, they can be processed by the standard GNSS correlators. However, a hypothetical difficulty can be caused by side correlation peaks.

As the previous paragraph explains, *the simple E-L correlators are the basic building blocks of the correlators for more complex signals*. More details are in [2].

The input and output memory registers for control of the correlators and the other blocks are a part of the Universal Correlator IP, as well.

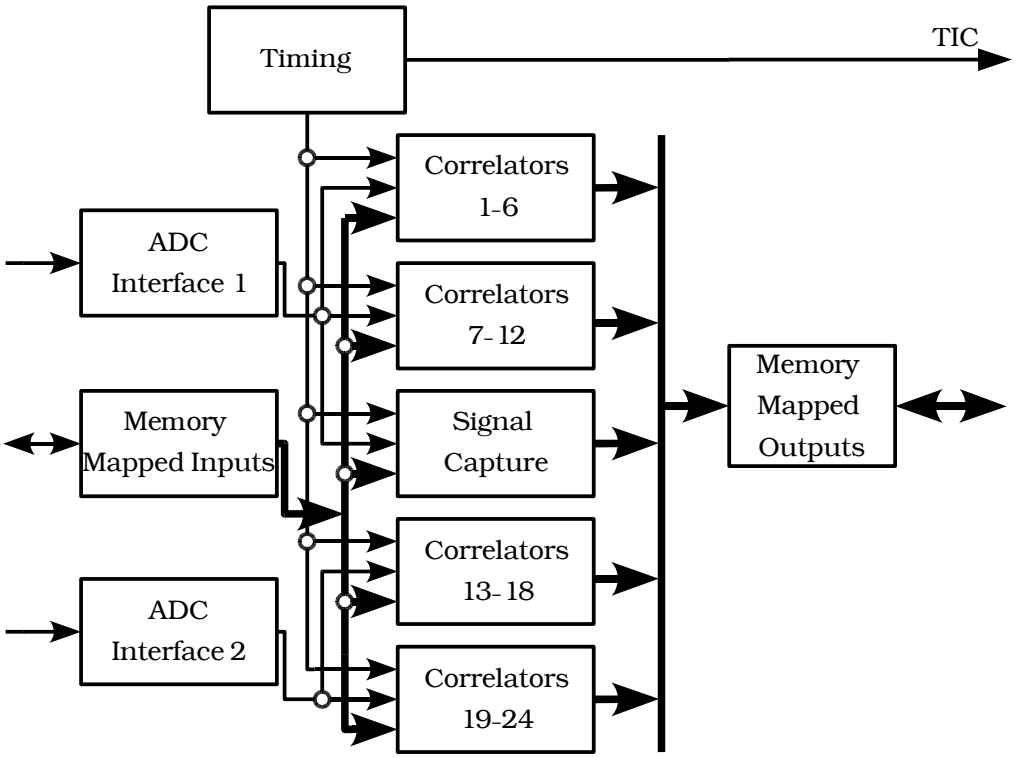

Figure 2: Universal Correlator IP

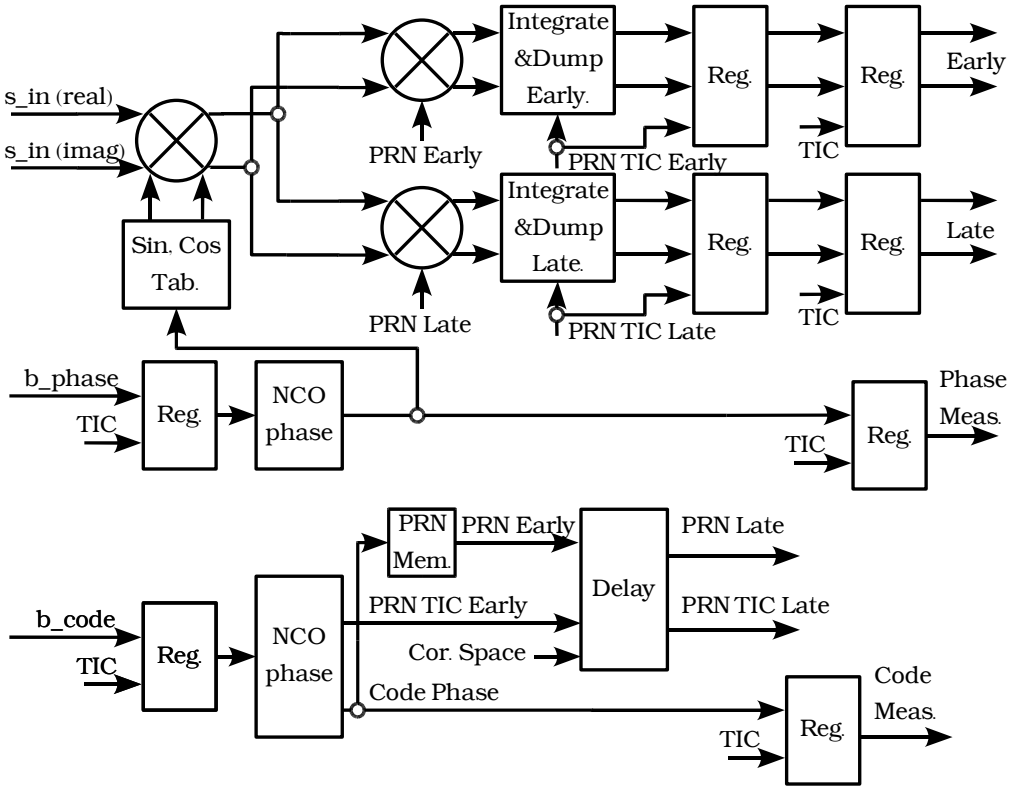

Figure 3: E-L correlator

2.1 Input Memory Mapped Registers

All the input registers of the FPGA processor are mapped to the Universal Correlator IP Input memory space (Table 1). As the address decoder does not respect all the address signals, the registers are repeated in the address space many times.

Note. Writing to the addresses that are not specify in Table 1 can cause an unpredictable behavior!

2.1.1 NCO Control Registers

The NCO control registers control the frequency of the Numerical Controlled Oscillators for generation of the signals for carrier frequency compensation (*NCO phase*) of the input signal and for the Pseudo Random Noise (PRN) sequence timing (*NCO code*). Mapping of the PRN phase and PRN code registers of the individual correlators is in Table 2.

Address	Content	Note
0x00000 ÷ 0x000FC	NCOs control registers	Write only
0x08000	Correlator control register	Read/Write
0x08004	DMA write address register (see Subsection 4)	Write only
0x08008	Correlator space register	Read/Write
0x0800C	I2C control register (see Subsection 3)	Write only
0x10000 ÷ 0x13FFC	PRN memory for correlators 1-6	Write only
0x14000 ÷ 0x17FFC	PRN memory for correlators 7-12	Write only
0x18000 ÷ 0x1BFFC	PRN memory for correlators 13-18	Write only
0x1C000 ÷ 0x1FFFC	PRN memory for correlators 19-24	Write only

Table 1. Input memory space organization

Address	Content
0x00000	Correlator 1. NCO code control word
0x00004	Correlator 1. NCO phase control word
0x00008	Correlator 7. NCO code control word
0x0000C	Correlator 7. NCO phase control word
0x00010	Correlator 2. NCO code control word
0x00014	Correlator 2. NCO phase control word
0x00018	Correlator 8. NCO code control word
0x0001C	Correlator 8. NCO phase control word
0x00020	Correlator 3. NCO code control word
0x00024	Correlator 3. NCO phase control word
0x00028	Correlator 9. NCO code control word
0x0002C	Correlator 9. NCO phase control word
0x00030	Correlator 4. NCO code control word
0x00034	Correlator 4. NCO phase control word
0x00038	Correlator 10. NCO code control word
0x0003C	Correlator 10. NCO phase control word
0x00040	Correlator 5. NCO code control word
0x00044	Correlator 5. NCO phase control word
0x00048	Correlator 11. NCO code control word
0x0004C	Correlator 11. NCO phase control word
0x00050	Correlator 6. NCO code control word
0x00054	Correlator 6. NCO phase control word
0x00058	Correlator 12. NCO code control word
0x0005C	Correlator 12. NCO phase control word
0x00060-0x0007C	Not used
0x00080	Correlator 13. NCO code control word
0x00084	Correlator 13. NCO phase control word
0x00088	Correlator 19. NCO code control word
0x0008C	Correlator 19. NCO phase control word

0x00090	Correlator 14, NCO code control word
0x00094	Correlator 14, NCO phase control word
0x00098	Correlator 20, NCO code control word
0x0009C	Correlator 20, NCO phase control word
0x000A0	Correlator 15, NCO code control word
0x000A4	Correlator 15, NCO phase control word
0x000A8	Correlator 2 1, NCO code control word
0x000AC	Correlator 2 1, NCO phase control word
0x000B0	Correlator 16, NCO code control word
0x000B4	Correlator 16, NCO phase control word
0x000B8	Correlator 22, NCO code control word
0x000BC	Correlator 22, NCO phase control word
0x000C0	Correlator 17, NCO code control word
0x000C4	Correlator 17, NCO phase control word
0x000C8	Correlator 23, NCO code control word
0x0008C	Correlator 23, NCO phase control word
0x000C0	Correlator 18, NCO code control word
0x000D4	Correlator 18, NCO phase control word
0x000D8	Correlator 24, NCO code control word
0x000DC	Correlator 24, NCO phase control word
0X000E0-0x000FC	Not used

Table 2. NCOs control registers mapping

2.1.2 Correlator Control Register

The Correlator control register is a 32-bit memory mapped input register for correlator control. The function of the individual bits is in Table 3. The register enables an interrupt and DMA transfer, controls the signal capture block, LED 1 and LED 3 on the receiver front panel.

The signal capture block can be programmed into various modes, see Table 4. We can capture 8-bit ADC signal samples from channel 1 or 2. Furthermore, we can capture 4-bit samples of both channels simultaneously. In the second case, we can select which ADC bits are captured.

Bit	Function
31	Irq&DMA enable
30÷12	Not used
11÷8	Signal capture control word
7÷3	Not used
1	LED 3
0	LED 1

Table 3. Correlator control register

Bit	Function
10xx	Channel 1, 8-bit resolution
11xx	Channel 2, 8-bit resolution
0x00	Channel 1&2, 4-bit resolution, ADC - bits 7÷4 of I&Q channels
0x01	Channel 1&2, 4-bit resolution, ADC - bits 6÷3 of I&Q channels
0x10	Channel 1&2, 4-bit resolution, ADC - bits 5÷2 of I&Q channels
0x11	Channel 1&2, 4-bit resolution, ADC - bits 4÷1 of I&Q channels

Table 4. Signal capture unit configuration

2.1.3 DMA Write Address Register

The DMA write address register serves for setup of the host's (PC) base address for the DMA transfer (see Chapters 4 , 5).

2.1.4 Correlator Space Register

The correlator space register (Figure 4) controls the correlator space, i. e. the time distance between early and late replicas. The timing of the early PRN code replica is directly controlled by the NCO code. The late replica is delayed by the time defined in Table 5. The Universal correlator IP enables to setup the correlator space of each sextuplet of the corraltors individually.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	Cor. 19-24			-	Cor. 13-18			-	Cor. 7-12			-	Cor. 1-6		

Figure 4: Correlator space register

Control bits	Correlator space in T_s
000	1
001	2
…	…
111	8

Table 5. Correlator space setup

2.1.5 PRN Memory

The PRN memory is a dual port memory for storage of the PRN codes. The host computer can write to this memory via the first port. The second port serves for reading of the PRN codes by the correlator PRN code generator. Each group of the correlators has its own PRN memory. The organization of the PRN memory is in Table 6.

Adress	Content								
	correlator	-	-	6/ 12/ 18/ 24	5/ 11/ 17/ 23	4/ 10/ 16/ 22	3/ 9/ 15/ 21	2/ 8/ 14/ 20	1/ 7/ 13/ 19
0x10000/ 0x14000/ 0x18000/ 0x1C000	Bit	31	30	29	28	27	26	25	24
		-	-	PRN bit 3	PRN bit 3	PRN bit 3	PRN bit 3	PRN bit 3	PRN bit 3
	Bit	23	22	21	20	19	18	17	16
		-	-	PRN bit 2	PRN bit 2	PRN bit 2	PRN bit 2	PRN bit 2	PRN bit 2
	Bit	15	14	13	12	11	10	9	8
		-	-	PRN bit 1	PRN bit 1	PRN bit 1	PRN bit 1	PRN bit 1	PRN bit 1
	Bit	7	6	5	4	3	2	1	0
		-	-	PRN bit 0	PRN bit 0	PRN bit 0	PRN bit 0	PRN bit 0	PRN bit 0
0x10004/ 0x14004/ 0x18004/ 0x1C004	Bit	31	30	29	28	27	26	25	24
		-	-	PRN bit 7	PRN bit 7	PRN bit 7	PRN bit 7	PRN bit 7	PRN bit 7
	Bit	23	22	21	20	19	18	17	16
		-	-	PRN bit 6	PRN bit 6	PRN bit 6	PRN bit 6	PRN bit 6	PRN bit 6
	Bit	15	14	13	12	11	10	9	8
		-	-	PRN bit 5	PRN bit 5	PRN bit 5	PRN bit 5	PRN bit 5	PRN bit 5
	Bit	7	6	5	4	3	2	1	0
		-	-	PRN bit 4	PRN bit 4	PRN bit 4	PRN bit 4	PRN bit 4	PRN bit 4
. . .	. . .								
0x127F4/ 0x167F4/ 0x1A7F4/ 0x1E7F4	Bit	31	30	29	28	27	26	25	24
		-	-	-	-	-	-	-	-
	Bit	23	22	21	20	19	18	17	16
		-	-	-	-	-	-	-	-
	Bit	15	14	13	12	11	10	9	8
		-	-	PRN bit 10229	PRN bit 10229	PRN bit 10229	PRN bit 10229	PRN bit 10229	PRN bit 10229
	Bit	7	6	5	4	3	2	1	0
		-	-	PRN bit 10228	PRN bit 10228	PRN bit 10228	PRN bit 10228	PRN bit 10228	PRN bit 10228

Table 6: PRN memory organization

2.1 Output Memory Mapped Registers

The output memory mapped registers serve for the universal correlator measurement result transfer to the host PC computer. The organization of this memory is in Table 7. There are two input registers mapped - Correlator control register and Correlator space register for verification purposes. The address decoder does not process all the address signals, therefore the registers are repeated many time outside the addresses.

Address	Content	Note
0x0000 ÷ 0x7CFC	Signal capture memory	Read only
0x7D00 ÷ 0x7DFC	NCOs output registers	Read only
0x7E00 ÷ 0x7E7C	Correlators output registers 1-12	Read only
0x7E80 ÷ 0x7EFC	Correlators output registers 13-24	Read only
0x7F00	Correlator control register	Read/Write
0x7F08	Correlator space register	Read/Write
0x7F10	TIC counter register	Read only
0x7F18	I2C status register (see subsection 3)	Read only

Table 7. Output memory space organization

2.1.1 Signal Capture Memory

The signal capture memory consists of two pages of 16000 memory cells. The size of each cell is 16 bits. Each page accommodates 800 µs of the raw signal. The organization of this memory is in Table 8. The content of each cell depends on signal acquisition mode that is defined in Signal capture control word (Table 9).

Address	Content	
	Bits 31 ÷ 16	Bits 15 ÷ 0
0x0000	Cell 1	Cell 0
0x0004	Cell 3	Cell 2
:	:	:
0x7CFC	Cell 15999	Cell 15998

Table 8. Signal capture memory organization

Single channel (8 bits samples)			
Bits 15 ÷ 8		Bits 7 ÷ 0	
Sample Q (8 bits)		Sample I (8 bits)	
Dual Channels (4-bit samples)			
Bits 15 ÷ 12	Bits 11 ÷ 8	Bits 7 ÷ 4	Bits 3 ÷ 0
Channel 2		Channel 1	
Sample Q (4 bits)	Sample I (4 bits)	Sample Q (4 bits)	Sample I (4 bits)

Table 9. Cell content

2.1.1 NCOs Output Registers

The NCOs output registers serve for presentation of the correlators code and phase measurements. The content of the code and phase NCOs is reduced to 32 bits and sampled by the TIC signal and saved to the NCOs output registers (Table 10).

Addr.	Content
0x7D00	Correlator 1 code measurement
0x7D04	Correlator 1 phase measurement
0x7D08	Correlator 7 code measurement
0x7D0C	Correlator 7 phase measurement
0x7D 10	Correlator 13 code measurement
0x7D 14	Correlator 13 phase measurement
0x7D 18	Correlator 19 code measurement
0x7D 1C	Correlator 19 phase measurement
0x7D20	Correlator 2 code measurement
0x7D24	Correlator 2 phase measurement
0x7D28	Correlator 8 code measurement
0x7D2C	Correlator 8 phase measurement
0x7D30	Correlator 14 code measurement
0x7D34	Correlator 14 phase measurement
0x7D38	Correlator 20 code measurement
0x7D3C	Correlator 20 phase measurement
0x7D40	Correlator 3 code measurement
0x7D44	Correlator 3 phase measurement
0x7D48	Correlator 9 code measurement
0x7D4C	Correlator 9 phase measurement
0x7D50	Correlator 15 code measurement
0x7D54	Correlator 15 phase measurement
0x7D58	Correlator 21 code measurement
0x7D5C	Correlator 21 phase measurement
0x7D60	Correlator 4 code measurement
0x7D64	Correlator 4 phase measurement
0x7D68	Correlator 10 code measurement
0x7D6C	Correlator 10 phase measurement
0x7D70	Correlator 16 code measurement

0x7D74	Correlator 16 phase measurement
0x7D78	Correlator 22 code measurement
0x7D7C	Correlator 22 phase measurement
0x7D80	Correlator 5 code measurement
0x7D84	Correlator 5 phase measurement
0x7D88	Correlator 11 code measurement
0x7D8C	Correlator 11 phase measurement
0x7D90	Correlator 17 code measurement
0x7D94	Correlator 17 phase measurement
0x7D98	Correlator 23 code measurement
0x7D9C	Correlator 23 phase measurement
0x7DA0	Correlator 6 code measurement
0x7DA4	Correlator 6 phase measurement
0x7DA8	Correlator 12 code measurement
0x7DAC	Correlator 12 phase measurement
0x7DB0	Correlator 18 code measurement
0x7DB4	Correlator 18 phase measurement
0x7DB8	Correlator 24 code measurement
0x7DBC	Correlator 24 phase measurement
0x7DC0-0x7DFC	Not used

Table 10. NCOs output registers

2.1.2 Correlators Output Registers

The Correlators output registers serve for presentation of the correlation results. The correlators' integrator outputs are sampled at the end of the PRN code and are stored in correlator's result registers. These registers are further resampled by the TIC signal and stored to the correlators output memory registers. The procedure is based on the usage of two memory pages.

Note. In some cases, the early branch of the E-L correlator can be sampled before the TIC signal and the late branch can be sampled after the TIC signal. After resampling by the TIC signal, the host computer has available only the early branch correlator outputs and the late branch correlator outputs will be available after the next TIC signal. This exception must be handled by the software!

The correlator's output memory had to be divided into two parts, one for correlators No. 1 – 12 and the second one for correlators No. 13 – 24. This solution was used due to the FPGA implementation constrains. The organization of this memory is in Table 11.

Addr.	Content		
0x7E00 / 0x7E80	bits	31 - 16	15 - 0
		Correlator 1 / 13, Early imag.	Correlator 1 / 13, Early real
0x7E04 / 0x7E84	bits	31 - 16	15 - 0
		Correlator 1 / 13, Late imag.	Correlator 1 / 13, Late real
0x7E08 / 0x7E88	bits	31 - 16	15 - 0
		Correlator 7 / 19, Early imag.	Correlator 7 / 19, Early real
0x7E0C / 0x7E8C	bits	31 - 16	15 - 0
		Correlator 7 / 19, Late imag.	Correlator 7 / 19, Late real
0x7E10 / 0x7E90	bits	31 - 16	15 - 0
		Correlator 2 / 14, Early imag.	Correlator 2 / 14, Early real
0x7E14 / 0x7E94	bits	31 - 16	15 - 0
		Correlator 2 / 14, Late imag.	Correlator 2 / 14, Late real
0x7E18 / 0x7E98	bits	31 - 16	15 - 0
		Correlator 8 / 20, Early imag.	Correlator 8 / 20, Early real
0x7E1C / 0x7E9C	bits	31 - 16	15 - 0
		Correlator 8 / 20, Late imag.	Correlator 8 / 20, Late real
0x7E20 / 0x7EA0	bits	31 - 16	15 - 0
		Correlator 3 / 15, Early imag.	Correlator 3 / 15, Early real
0x7E24 / 0x7EA4	bits	31 - 16	15 - 0
		Correlator 3 / 15, Late imag.	Correlator 3 / 15, Late real
0x7E28 / 0x7EA8	bits	31 - 16	15 - 0
		Correlator 9 / 21, Early imag.	Correlator 9 / 21, Early real
0x7E2C / 0x7EAC	bits	31 - 16	15 - 0
		Correlator 9 / 21, Late imag.	Correlator 9 / 21, Late real
0x7E30 / 0x7EB0	bits	31 - 16	15 - 0
		Correlator 4 / 26, Early imag.	Correlator 4 / 26, Early real
0x7E34 / 0x7EB4	bits	31 - 16	15 - 0
		Correlator 4 / 26, Late imag.	Correlator 4 / 26, Late real
0x7E38 / 0x7EB8	bits	31 - 16	15 - 0
		Correlator 10 / 22, Early imag.	Correlator 10 / 22, Early real
0x7E3C / 0x7EBC	bits	31 - 16	15 - 0
		Correlator 10 / 22, Late imag.	Correlator 10 / 22, Late real
0x7E40 / 0x7EC0	bits	31 - 16	15 - 0
		Correlator 5 / 17, Early imag.	Correlator 5 / 17, Early real

0x7E44 / 0x7EC4	bits	31 - 16	15 - 0
		Correlator 5 / 17, Late imag.	Correlator 5 / 17, Late real
0x7E48 / 0x7EC8	bits	31 - 16	15 - 0
		Correlator 11 / 23, Early imag.	Correlator 11 / 23, Early real
0x7E4C / 0x7ECC	bits	31 - 16	15 - 0
		Correlator 11 / 23, Late imag.	Correlator 11 / 23, Late real
0x7E50 / 0x7ED0	bits	31 - 16	15 - 0
		Correlator 6 / 18, Early imag.	Correlator 6 / 18, Early real
0x7E54 / 0x7ED4	bits	31 - 16	15 - 0
		Correlator 6 / 18, Late imag.	Correlator 6 / 18, Late real
0x7E58 / 0x7ED8	bits	31 - 16	15 - 0
		Correlator 12 / 24, Early imag.	Correlator 12 / 24, Early real
0x7E5C / 0x7EDC	bits	31 - 16	15 - 0
		Correlator 12 / 24, Late imag.	Correlator 12 / 24, Late real
0x7E60-0x7E7C / 0x7EE0-0x7EFC	Not used		

Table 11. Correlators output registers

2.1.1 Correlator Control Register

The correlator control register is a read/write register described in Subsection 2.1.2.

2.1.2 Correlator Space Register

The correlator space register is a read/write register described in Subsection 2.1.4.

2.1.3 TIC Counter Register

The TIC counter register presents state of the 16-bit TIC counter (LSB bits). The MSB bits are zero.

2.1.4 I2C Status Register

The I2C status register is an output register of the I2C controller, see Chapter 3 .

2.2 NCO Code

The NCO code serves for timing of the PRN replica. The NCO code is programmed as an unsigned 40-bit accumulator, which is controlled via NCO code control register b_{code}. The 14 MSB bits represent the PRN chip number and the 26 LSB bits represent the

fractional part of the chip. Because the length of the PRN code is not equal to a power of two, the accumulator overflow must be specially treated. The 14 MSB bits are automatically cleared when these bits are equal to predefined threshold `prn_length`. The default value of `prn_length` is 10 230 and can be modified in VHDL code to any value between 1 and 2^{14} to be able to fit the length of the PRN code to GLONASS for example.

The applied accumulator limitation technique does not operate properly when the last PRN chip is omitted. This impractical situation can occur when b_{code} value exceeds 2^{26}. In this case the PRN chip duration is longer then T_s. The PRN chip rate is given

$$f_{chip} = \frac{1}{T_s} \frac{b_{code}}{2^{26}}.$$

The code measurement output register is reduced to 32 bits. The 14 MSB bits of the code measurement represent PRN chip number and the 18 LSB bits represent the fractional part.

Note. The code measurement of the correlator outputs represent the code phase of the early PRN replica in the TIC event. The true code measurement value (phase of not implemented prompt branch) is delayed of one-half of the correlator space and lies exactly in the middle of the early and late replica phases! This code measurement shift must be compensated by the software!

For short codes like GPS L1 C/A we recommend to repeat chips in the PRN memory 10 times and set `prn_length` to 10230. The reason of this recommendation is to extend the resolution of NCO code 10 times.

2.3 NCO Phase

The NCO phase generates heterodyne signals for the carrier frequency residue compensation. The NCO phase is programmed as a signed 40-bit accumulator which accumulates NCO phase control word b_{phase}.

Organization of the accumulator is as follows. The 32 LSB bits represent fractional part of the carrier phase and the 8 MSB bits count carrier cycles. One cycle (2π radians) corresponds to 2^{32}. The frequency of the NCO phase is given

$$f_{NCOphase} = \frac{1}{T_s}\frac{b_{phase}}{2^{32}}.$$

The control word b_{phase} is a signed variable, which is coded as twos complement to be able to generate positive and negative frequencies. The phase measurement output register is reduced to 32 bits, see Subsection 15. The 8 LSB bits are ignored.

3 I2C Controller

The I2C controller is a simple master controller for the receivers' I2C control via I2C bus. This controller has implemented a *single register read* and a *single register write* operations (Figure 5. 6). Sequential operations are not implemented. The controller is controlled via `i2c_control` (write) register (Table 12) and `i2c_status` (read) register (Table 13).

The transaction is started on the raising edge of the `i2c_start` bit. After the transaction start the controller operates automatically. The communication (read or write I2C transaction) on the I2C bus is indicated by the `i2c_busy` flag. Note. The processor must not change the content of the `i2c_status` register during transaction! The error during transaction is indicated by the flag `i2c_error` bit. The error bit is automatically set to zero after the start of the next read or write transaction.

The read data are saved in the `i2c_status` register. The read data is valid after the read transaction finishes, which is indicated by the `i2c_busy` flag.

start	device addr. for write	register addr.	written data	stop

Figure 5: Register write operation

start	device addr. for write	register addr.	start	device addr. for read	read data	stop

Figure 6: Register read operation

Bits	Name	Function
31-26	-	Not used
25	`i2c_wr`	1 – register write, 0 – register read
24	`i2c_start`	Raising edge initiates I2C communication
23(MSB) – 16(LSB)	device addr.	IC address: the LSB bit, which differentiates read and write transaction is controlled automatically.
15(MSB) - 8(LSB)	reg. addr.	Read or write register address.
7(MSB) - 0(LSB)	data (write)	Written data (for write operation only)

Table 12. `i2c_control` register

Bits	Name	Function
31-10	-	Not used, (0)
9	`i2c_error`	Inserted when an I2C opperation error has occurred. Automatically zero after start of the next I2C transaction.
8	`i2c_bussy`	Indicates that the I2C opperation is in progress
7(MSB) - 0(LSB)	data (read)	Read data by the last read operation

Table 13. `i2c_status` register

4 PCI Express Interface IP

The PCI Express Interface IP transforms (PCIeIIP) Transaction Layer Packets (TLP) to memory read and memory write operations and generates Message Send Interrupt (MSI). A part of this block is a Direct Memory Access (DMA) controller.

The PCIe has implemented

- 32 and 64-bit addressing.
- single DW memory write request reception and processing.
- single DW memory read request reception and processing.
- single DW memory read completion generation.
- 32-DW memory write request generation.
- DMA controller for data transfer form the device to the host.
- MSI interrupt.

The DMA controller automatically transfers data form the device (FPGA) to the host (PC). This transfer is initiated by the TIC signal (Figure 7). At the end of the DMA transfer, the MSI interrupt is generated. The 32-DW (128 bytes) memory write request packet is used because this transaction length is implemented in all PCI Express chip sets. The number of TPL packets (`DMA_TLP_NO` = 255) is setup in VHDL code as well as the DMA device address space. The DMA controller transfers data from the device addresses 0x0000 ÷ 128 * `DMA_TLP_NO`. The host (PC) base address is setup in DMA write address register (write). The DMA and MSI interrupt are enabled by the `Irq&DMA` enable bit in Correlator control register.

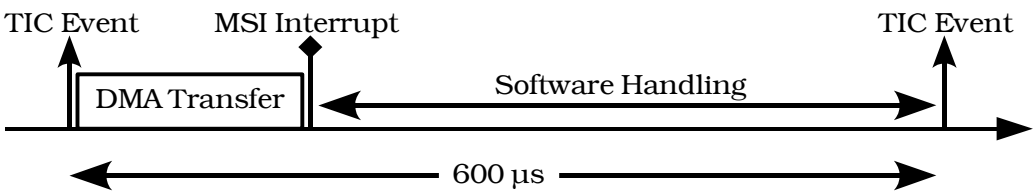

Figure 7: DMA communication

5 PCI Express IP

The PCI Express IP (PCIe) block is a standard Xilinx IP for the PCIe interface. This block does not need any software control.

Setup:

- BAR 0: 1MegaBytes: Memory,
- Wonder ID: 0x10EE (Xilinx Wonder ID),
- Device ID: 0x0007,
- Revision ID: 0x00,
- MSI interrupt: one vector.

6 PLL125

The PLL 125 MHz is a standard Xilinx block for clock synthesis. It generates 125 MHz clock signal for the PCIe IP from the 100 MHz ExpressCard clock. This block does not need any software control.

Bibliography

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